

# A SURVEY ON WAVELET TRANSFORM TECHNIQUES J. Vinoth Kumar\* & Dr. C. Kumar Charlie Paul\*\*

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#### **Abstract:**

Computational tool for a variety of signal and image processing applications do exist and the wavelet transform has become a useful tool among them. Smaller files are important for storing images using less memory and for transmitting images faster and more reliably and hence the wavelet transform is useful for the compression of digital image files. Compressing digitally scanned fingerprint images is done by the FBI using wavelet transforms. For compressing images acquired by their 18 cameras, NASA's Mars Rovers used wavelet transforms. The special requirements of deep-space communication to meet the wavelet-based algorithm implemented in software onboard the Mars Rovers is designed. Based on wavelet transforms JPEG2K (the newer JPEG image file format) compression technique is designed. 'Cleaning' signals and 'Images' are also done using Wavelet transforms which are also useful for reducing unwanted noise and blurring. Based on wavelet and wavelet-like transforms, some algorithms for processing astronomical images, for example do exist.

**Key Words:** Wavelet Transform, Image Processing, Image Compression & Pipelining **1. Introduction:** 

The wavelet transform, and how it is effective for noise reduction is illustrated by this Quick Study and it briefly describes several improvements of the basic wavelet transform and basic noise reduction method used in the illustration. What the wavelet transforms is, and the algorithms for processing a signal after its wavelet transform has been computed are described. Wavelet transform consists of two basic types of transformations. Easily reversible (invertible) is the nature of the one type of wavelet transform designed. It is the transform in which the original signal can be easily recovered after it has been transformed. Image compression and cleaning (noise and blur reduction) put these kinds of transforms into utilization. Typically the wavelet representation is then modified appropriately after computation of the wavelet transform and then the wavelet transform is reversed (inverted) to obtain a new image. Signal analysis is the use of the second type of the wavelet transform. The transform is used to detect faults in machinery from sensor measurements, to study EEG or other biomedical signals and to determine how the frequency content of a signal evolves over time. Modified form of the original signal is not needed in these cases and the wavelet transform need not be inverted. The inversion of the wavelet transform is possible but it requires a lot of computation time in comparison with the first type of wavelet transform. Those wavelet transforms that are easily invertible will be the focus of this short survey.

## 2. Literature Review:

The most promising tool for various applications such as image compression, bioinformatics, pattern recognition and video processing and many more) is the discrete wavelet transforms (DWT). Better image quality, coding efficiency, noise immunity are the suitable features of DWT making it more efficient as compared to Discrete Cosine Transform. VLSI implementation of DWT is done using convolution-based scheme and lifting-based scheme. Simplified computation, parallel and fast implementation, in place computation, integer to integer mapping, low memory requirement [1], [2], are the powerful features of liftingbased scheme which has more advantages compared to convolution-based scheme. Longer and critical delays for direct mapped architecture are the disadvantage of the lifting based scheme. Additionally it also needs extra memory for rearranging interleaved intermediate outputs, hence taking a toll on its hardware efficiency. The key points determining the efficiency of the architecture are the memory requirement and critical path delay. Intermediate results for column processing as soon as possible, with a transposition buffer of size 2.5N are proposed by Mohanty et al [3]. The architecture with parallel processed systolic arrays to make the intermediate results available immediately. Memory is divided into two categories. Temporal memory is used to store partial results and transposition memory is used to store intermediate outputs. The outputs of the previous step are used as inputs for the current step except the first step in the lifting based scheme. Addition and multiplication operation are the constituent of each lifting step. Critical path delay is contributed by the adder delay T<sub>a</sub> and multiplication delay T<sub>m</sub>. Temporal memory of large size is required to reduce the path delay. Increased size of transposition memory is the result if pipelining is used to reduce path delay. Architectures have been developed to achieve balance between path delay and memory requirement in recent years. To eliminate data transposition step between row and column processing Mohanty et al. [4] proposed architecture resulting into the small size of transposition memory. The block based scanning method is introduced by Cheng and Parhi et al. [5]. The

strip based scanning method for the first time is proposed by Chiu et al. [6]. Huang et al. [7] was the first to propose the Flipping method. The architecture to map last component with first component of same systolic array for column processing in a symmetric and cyclic manner was modified by Bhanu et al. [8]. Several parallel units in both row processor and column processor, achieving path delay of  $T_a + T_m$  with smaller size of the temporal memory of 3N has been implemented by Hu et at. [9]. The pipelined architecture with flipping method resulting in path delay of  $T_m$  only with the smaller transposition buffer is proposed by Zhang et at. [10]. The path delay of  $T_m$  only and smallest temporal memory of 2N with pipelined architecture is achieved by Darji et al. [11].

## 3. Future Enhancement and Conclusion:

2-D lifting-based DWT that are recently implemented with existing memory efficient architectures are studied compared and analyzed for arithmetic resources utilized, on chip memory consumed and computation time required for processing with different delays. Parallel scan, block-based scan and strip scan with parallel computation, flipping and pipelining techniques are some of the architectures that are presented. Study and implementation of multi-level decomposition of images for real time applications will be the purpose of the survey.

#### 4. References:

- 1. W. Sweldens, "The lifting scheme: A custom-design construction of biorthogonal wavelets," Appl. Comput. Harmon. Anal., Vol. 3, no. 2, pp. 186-200, Apr. 1996.
- 2. Daubechies and W. Sweldens, "Factoring wavelet transforms into lifting steps," J. Fourier Anal. Appl. Vol. 4, no. 3, pp. 247-269, 1998.
- 3. B. K. Mohanty and P. K. Meher, "Memory-efficient modular VLSI architecture for high-throughput and low-latency implementation of multilevel lifting 2-D DWT," iEEE Trans. Signal Process., vol. 59,no. 5,pp. 2072-2084, May 2011.
- 4. B. K. Mohanty, A. Mahajan, and P. K. Meher, "Area and power efficient architecture for high-throughput implementation of lifting 2-D DWT," JEEE Trans. Circuits Syst. ii, Exp. Briefs, vol. 59, no. 7, pp. 434--438, July 2012.
- 5. C. Cheng and K. K. Parhi, "High-speed VLSI implementation of 2- D discrete wavelet transform," iEEE Trans. Signal Process., vol. 56,no. I,pp. 393-403,2008.
- 6. Chiu, K.-B. Lee, and c.-W. Jen, "Optimal data transfer and buffering schemes for JPEG2000 encoder," in Proc. Signal Process. Syst., pp. 177-182, 2003.
- C.-T. Huang, P.-C.Tseng, and L.-G. Chen, "Flipping structure: An efficient VLSI architecture for lifting-based discrete wavelet transform," IEEE Trans. Signal Process., vol. 52, no. 4, pp. 1080-1089, Apr. 2004.
- 8. N. U. Bhanu and A. Chilambuchelvan, "High-speed systolic VLST architecture for 2-D forward lifting-based DWT", Arab J Sci Eng 39, pp. 6125-6135, June 2014.
- 9. Y. Hu and C. C. Jong, "A memory-efficient scalable architecture for lifting-based discrete wavelet transform," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 60, no. 8,pp. 502-506, August 2013.
- 10. W. Zhang, Z. Jiang, Z. Gao, and Y. Liu, "An efficient VLST architecture for lifting-based discrete wavelet transform," IEEE Trans. Circuits Syst. II, vol. 59, pp. 158-162, March 2012.
- 11. D. Darji and A. Limaye, "Memory efficient VLSI architecture for lifting-based DWT", 57th IEEE International Midwest Symposium on Circuits and Systems, pp. 189-192, 2014.